



## Hi3521/Hi3520A Hardware Design **Checklist**

Issue	03
Date	2013-01-21

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## **HiSilicon Technologies Co., Ltd.**

Address: Huawei Industrial Base  
Bantian, Longgang  
Shenzhen 518129  
People's Republic of China

Website: <http://www.hisilicon.com>

Email: [support@hisilicon.com](mailto:support@hisilicon.com)



## About This Document

### Purpose

This document describes the check items for Hi3521/Hi3520A solutions.

### Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3521	V100
Hi3520A	V100

### Intended Audience

This document is intended for:

- Technical support personnel
- Board hardware development engineers

### Change History

Updates between document issues are cumulative. Therefore, the latest document issue contains all updates made in previous issues.

#### Issue 03 (2013-01-21)

This issue is the third official release, which incorporates the following changes:

The descriptions of the Hi3520A are added.

1.4 Design Requirements on DDR Circuits

Requirements on DDR traces are modified.

1.5 Design Requirements on the SPI and NAND Flash



Requirements on the WP signal of the SPI flash are added.

## **Issue 02 (2012-11-30)**

This issue is the second official release, which incorporates the following changes:

### **Chapter 1 Checklist**

In section 1.16, the recommendation is changed to a requirement.

## **Issue 01 (2012-09-21)**

This issue is the first official release, which incorporates the following changes:

### **Chapter 1 Checklist**

In section 1.1, the requirements on the Hi3521 and Hi3520A DVDD10 are added, and the specifications of the beads for isolating the DVDD10 and DVDD33 power supplies from the PLL power are added.

Section 1.1.8 is added.

## **Issue 00B10 (2012-06-30)**

This issue is the first draft release.



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# 1 Checklist

## 1.1 Design Requirements on the Power Supply and GND

√	Items
	The core power pins DVDD10 connect to the 1.0 V digital power. A DC-DC power chip that provides 5 A or larger current is recommended for the Hi3521, and a DC-DC power chip that provides 4 A or larger current is recommended for the Hi3520A.
	Power supplies are powered on in the sequence of high voltage to low voltage. That is, the 3.3 V, 2.5 V, 1.5 V (or 1.8 V), and 1.0 V power supplies are powered on in sequence.
	The phase-locked loop (PLL) power pins VDD10_PLL1, VDD10_PLL2345, VDDREF10_PLL2345, AVDD33_PLL1, and AVDD33_PLL2345 are isolated from 1.0 V and 3.3 V power supplies by using 1000 $\Omega$ @100 MHz ferrite beads. In addition, 0.1 $\mu$ F capacitors are connected close to pins. For details, see the schematic diagram of the Hi3521 demo board and PCB.
	Ensure that the output voltage of power supplies meets the requirements of the Hi3521/Hi3520A when the ripple and noise occur. For details about the requirements on the power supply of each module, see the "Electrical Specifications" section in the <i>Hi3521/Hi3520A H.264 Codec Processor Data Sheet</i> .

## 1.2 Design Requirements on Clock Circuits of the Master Chip

√	Items
	A 24 MHz external clock is provided for the Hi3521/Hi3520A and the maximum deviation is $\pm 30$ ppm.



## 1.3 Design Requirements on Reset Circuits

√	Items
	The Hi3521/Hi3520A is reset by the low level. The low pulse width of the power-on reset signal is longer than 12 XIN crystal cycles.
	The Hi3521/Hi3520A watchdog is open drain (OD) output. When the watchdog is used, pull-up resistors are required. The 4.7 k $\Omega$ pull-up resistors are recommended.

## 1.4 Design Requirements on DDR Circuits

√	Items
	You are advised to connect the double-data rate (DDR) data signals DQS, DQ, and DM directly, because there is an internal on-die termination (ODT) and therefore no external serial resistors are required. For details, see the <i>Hi3521/Hi3520A Hardware Design User Guide</i> .
	DDR2 clock signals are connected in matched termination mode and a 100 $\Omega \pm 1\%$ resistor is recommended at the load end. DDR3 clock signals are connected according to the Thevenin's theorem, a 120 $\Omega \pm 1\%$ pull-up resistor is connected next to the load end to the 1.5 V power supply, and a 120 $\Omega \pm 1\%$ pull-down resistor connects to GND.
	The reference power supplies of the DDR2 and DDR3 are obtained by dividing the voltages of 1.8 V and 1.5 V power supplies respectively. Two 1% 1 k $\Omega$ (or smaller) voltage divider resistors are connected in serial to ensure optimum voltage.
	The trace width for the DDR VREF power is 20 mils or wider and the trace is isolated from other signals. Sufficient filtering capacitors connect to 1.5 V or 1.8 V power pins of the master chip and DDR. To be specific, at least one filtering capacitor is connected for two pins, and the DDR and the Hi3521/Hi3520A double-data rate controller (DDRC) interface shares a 1.5 V or 1.8 V power plane.
	The DDR signal traces are routed far away from the system crystal signal traces during printed circuit board (PCB) design and the traces have independent current return paths.
	You are advised to route the DDR trace with the same length as that for the Hi3521 demo board. For details, see the <i>Hi3521/Hi3520A Hardware Design User Guide</i> .



## 1.5 Design Requirements on the SPI Flash and NAND Flash

√	Items
	The NAND flash can boot only from chip select 0 (CS0). You are advised to connect 4.7 kΩ pull-up resistors to the RDY, CS, and WP signals of a NAND flash.
	The serial peripheral interface (SPI) flash can boot only from CS1. You are advised to connect 4.7 kΩ pull-up resistors to the CS0, CS1, and HOLD signals of an SPI flash. You are advised to connect a 4.7 kΩ pull-down resistor to the WP signal.

## 1.6 Design Requirements on I<sup>2</sup>C Circuits

√	Items
	Pull-up resistors connect to the inter-integrated circuit (I <sup>2</sup> C) signals SCL and SDA, because the signal pins are OD output. The impedance depends on the bus load.
	Note that the I <sup>2</sup> C addresses of the TW2867 and TW2960 are the same. The addresses of other I <sup>2</sup> C devices cannot conflict.

## 1.7 Design Requirements on the VI Interfaces, VO interfaces, and Video Interface Circuits

√	Items
	<p>The Hi3521/Hi3520A has one BT.656 output interface and three physical BT.1120 interfaces: VIU0, VIU1, and VOU1120.</p> <p>As 16-bit video input (VI) interfaces, VIU0 and VIU1 support external synchronization. Each interface can be divided into two BT.656 input interfaces. In this case, external synchronization is not supported.</p>
	<p>As the BT.1120 output interface, VOU1120 can connect to the high-definition multimedia interface (HDMI) physical layer (PHY) to output HDMI signals. VOU1120 and VOU656 can be multiplexed as an LCD interface to output 24-bit RGB signals. For details about the multiplexing relationship, see the <i>Hi3521/Hi3520A H.264 Codec Processor Data Sheet</i>.</p>
	<p>The Hi3521/Hi3520A has an HDMI PHY. That is, the Hi3521/Hi3520A can output HDMI signals directly. The HDMI module has a dedicated I<sup>2</sup>C interface. The HDMI_REXT pin connects to 51 kΩ and 6.8 kΩ resistors in parallel, and then to GND.</p>





√	Items
	The Hi3521/Hi3520A has two video digital-to-analog converters (VDACs). The first VDAC has three pins: VDAC0_IOUT0, VDAC0_IOUT1, and VDAC0_IOUT2. VDAC0_IOUT0 and VDAC0_IOUT1 output composite video broadcast signals (CVBSs), but VDAC0_IOUT2 has no output. The pins must connect to 75 $\Omega$ resistors, and then to GND. Note the matched impedance during design.
	The second VDAC has three signal output pins: VDAC1_IOUT0, VDAC1_IOUT1, and VDAC1_IOUT2. The three pins can output VGA signals. Note that the level of the I <sup>2</sup> C signal of the video grid array (VGA) interface must be converted.
	The values of the external resistors and capacitors of the VDACs are determined based on the <i>Hi3521/Hi3520A Hardware Design User Guide</i> .

## 1.8 Design Requirements on I<sup>2</sup>S Audio Circuits

√	Items
	The Hi3521/Hi3520A has three inter-IC sound (I <sup>2</sup> S) interfaces SIO0–SIO2. SIO0–SIO1 interfaces support only inputs, and SIO2 supports input and output (six pins).
	SIO2 is used to input and output I <sup>2</sup> S signals during talkback.



## 1.9 Design Requirements on the SPI Control Interface Circuits

√	Items
	The Hi3521/Hi3520A SPI control interface provides the SPI CLK, SDO, and SDI signals and four CSs (active low).
	If the SPI connects to multiple devices such as GV7601s that are connected in daisy chain mode, the delay for each device caused by data transfer is taken into account when the working frequency of the SPI clock signal SCLK is configured.

## 1.10 Design Requirements on USB Circuits

√	Items
	The Hi3521/Hi3520A provides two universal serial bus (USB) interfaces: USB0 and USB1.
	You are advised to connect USB_REXT to a $43.2\ \Omega \pm 1\%$ resistor, and then to GND, and place the resistor close to the Hi3521/Hi3520A.
	USB differential traces do not cross plane splits and are surrounded with GND traces. The impedance of each USB differential trace is $90\ \Omega \pm 10\%$ .

## 1.11 Design Requirements on SATA Circuits

√	Items
	The Hi3521/Hi3520A provides two serial advanced technology attachment 2.6 (SATA 2.6) interfaces: SATA0 and SATA1.
	The 10 nF surface mounting technology (SMT) capacitors are connected in series close to the SATA socket on the four SATA differential traces (including the TX and RX traces), and the differential impedance of each trace is less than or equal to $100\ \Omega$ .
	The SATA module has 1.0 V and 2.5 V power pins. The power pins must be isolated by using ferrite beads and filtering capacitors are connected. In addition, SATA_REXT connects to a $191\ \Omega \pm 1\%$ external resistor, and then to GND.



## 1.12 Design Requirements on ETH Circuits

√	Items
	As the management data input/output (MDIO) pin is OD output, you are advised to connect a 4.7 kΩ pull-resistor to the MDIO pin. Note that the MDCK pin is multiplexed as the pin for JTAG_SEL0, and the branch trace must be shorter than or equal to 300 mils.
	If the Ethernet PHY works in media independent interface (MII) mode, the associated clock RGMII_TXCK for data output is used. If the Ethernet PHY works in RGMII mode, the associated clock RGMII_TXCKOUT for data output is used.

## 1.13 Design Requirements on JTAG and System Control Circuits

√	Items
	4.7 kΩ pull-up resistors connect to TDI, TDO, and TMS pins; a 1 kΩ pull-down resistor connects to the TCK pin; a 10 kΩ pull-down resistor connects to the TRST pin. Note that the TRST pin can connect to a pull-up resistor for connecting to other emulators.
	The TESTMODE pin connects to a 10 kΩ pull-down resistor, and then to GND.

## 1.14 Design Requirements on SD Card Circuits

√	Items
	The Hi3521/Hi3520A does not provide a dedicated SD card interface. This interface is multiplexed with VOU656. For details, see the <i>Hi3521/Hi3520A H.264 Codec Processor Data Sheet</i> .
	You are advised to power on or power off the power supply of the SD card by using the MOSFET. The control signal is active high.
	You are advised to connect data and command signals to 4.7 kΩ resistors, and then to VCC_SDIO.
	SDIO_CDATA3 does not support card detection.



## 1.15 Design Requirements on UART Circuits

√	Items
	The debugging serial port is connected. Universal asynchronous receiver transmitter 0 (UART0) is used for debugging by default.

## 1.16 Design Requirements on the eFUSE Module

√	Items
	Ensure that the VDD25_EFUSE pin is connected to a 4.7 kΩ pull-down resistor and then to the GND.

## 1.17 Design Requirements on Heat Dissipation

√	Items
	The product structure is considered during the heat dissipation design. The size of the heat dissipation layer is as large as possible when the space is sufficient. You are advised to dissipate the heat of the main chip by installing a thermal pad between the chip and the product cover to ensure operation reliability. For details, see the description of heat dissipation design in the <i>Hi3521/Hi3520A Hardware Design User Guide</i> .

## 1.18 Design Requirements on the HDMI

√	Items
	The 1.0 V power pins K21 and L21 of the HDMI (AVDD10_HDMI) must be isolated from the 1.0 V power by using 1000 Ω@100 MHz ferrite beads, and 100 μF and 0.1 μF filtering capacitors are connected after the beads. For details, see the schematic diagram of the demo board.